ABSTRACT

Port priorities are defined on a 32-bit word, 16-bit half-word, and 8-bit byte basis to control the write enable signals to a compute register file (CRF). With a manifold array (ManArray) reconfigurable register file, it is possible to have double-word 64-bit and single word 32-bit data-type instructions mixed with other double-word, single-word, half-word, or byte data-type instructions within the same very long instruction word (VLIW). By resolving a write priority conflict on the byte, half-word, or word that is in conflict during the VLIW execution, it is possible to have partial operations complete that provide a useful function. For example, a load half-word to the half-word H0 portion of a 32-bit register R0 can have priority to complete its operation while a 64-bit shift of the register pair R0 and R1 will complete its operation on the non-conflicting half-word portions of the 64-bit register R0 and R1. Other unique capabilities result from the present approach to assigning port priorities that improve the performance of the ManArray indirect VLIW processor.